Abstract

Electronic Devices Having Wireless Transceivers with Reference Clock Selection

An electronic device may include wireless circuitry with first and second mixers on a signal path for converting a signal using first and second clock signals via high side injection (HSI) or low side injection (LSI). A first phase-locked loop (PLL) may generate the first clock signal and a second PLL may generate the second clock signal. A switch may couple the first PLL to a reference oscillator when LSI is used and may couple the first PLL to a third PLL when HSI is used. The third PLL may generate a second reference signal based on a first reference signal from the reference oscillator. The second PLL may generate the second clock signal based on the output of the third PLL. This may serve to may minimize phase noise even as the mixers switch between HSI and LSI.
Figure 1